EXHIBIT 5 – Part 1

(12) United States Patent Falster

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*May 22, 2001

(54)	SILICON ON INSULATOR STRUCTURE
	FROM LOW DEFECT DENSITY SINGLE
	CRYSTAL SILICON

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(*) Notice:

This patent issued on a continued prosecution application filed under 37 CFR 1.53(d), and is subject to the twenty year patent term provisions of 35 U.S.C. 154(a)(2).

Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: 09/387,288

(22) Filed: Aug. 31, 1999

Related U.S. Application Data

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(51)	Int. Cl. ⁷	H01L 29/06; H01L 27/01;
		H01L 27/12; H01L 31/0392
(52)	U.S. Cl.	257/618 ; 257/347; 257/913

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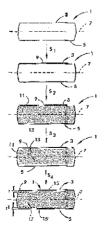
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(57) ABSTRACT

The present invention relates to a silicon on insulator ("SOI") structure having a low defect density device layer and, optionally, a handle wafer having improved gettering capabilities. The device layer comprises a central axis, a circumferential edge, a radius extending from the central axis to the circumferential edge, and a first axially symmetric region which is substantially free of agglomerated intrinsic point defects. Additionally, the present invention is directed to such a SOI structure which has a Czochralski single crystal silicon handle wafer which is capable of forming an ideal, non-uniform depth distribution of oxygen precipitates upon being subjected to the heat treatment cycles of essentially any arbitrary electronic device manufacturing process.

40 Claims, 35 Drawing Sheets



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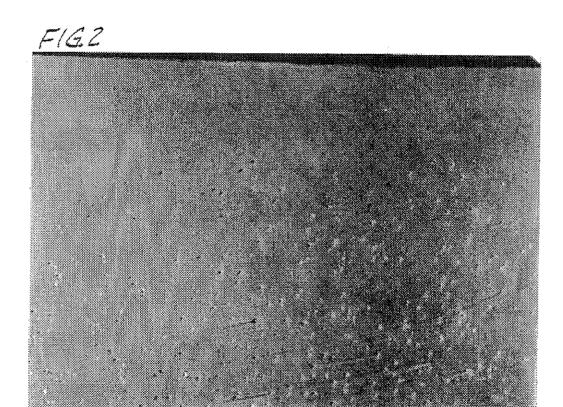
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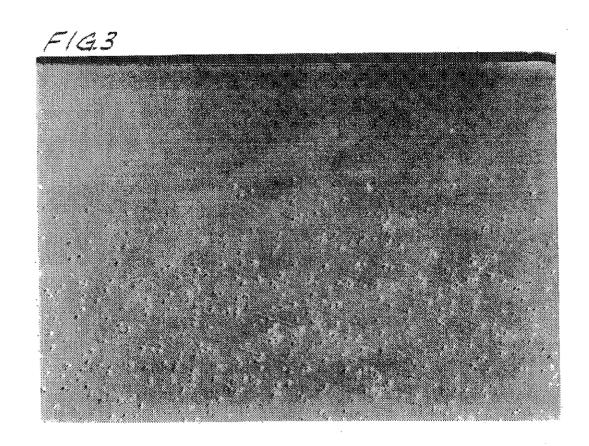
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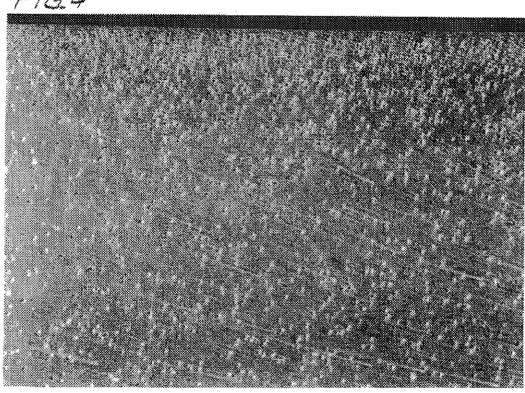


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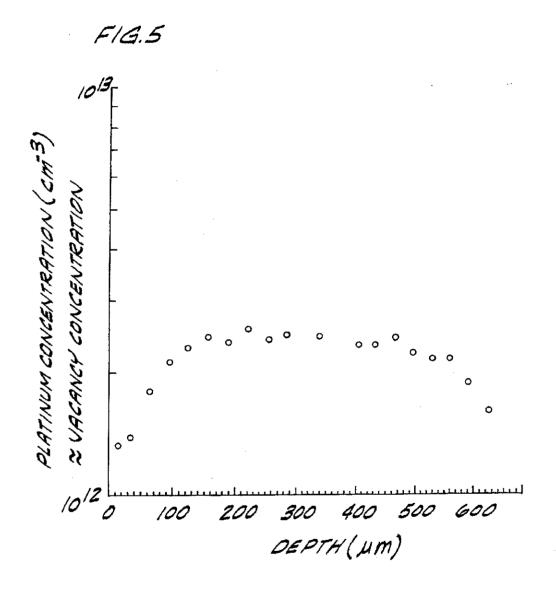
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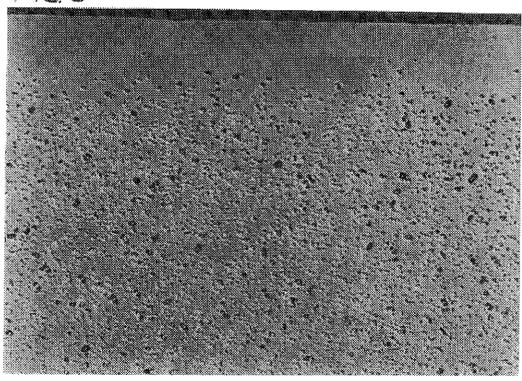
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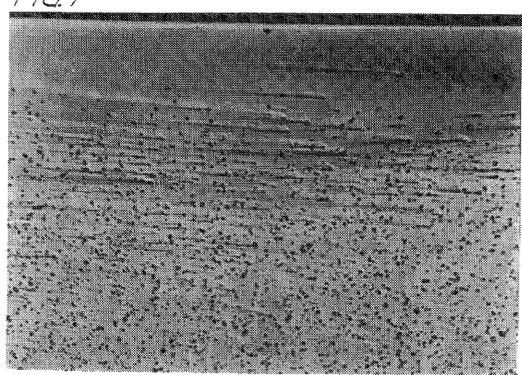
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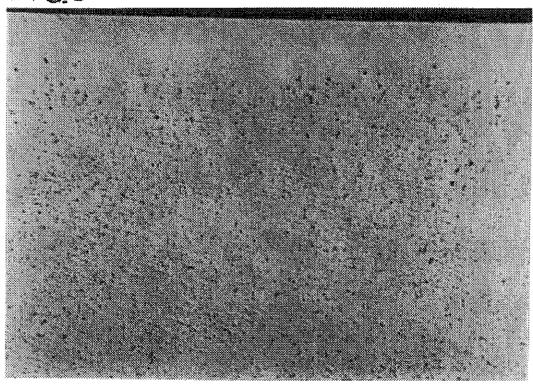
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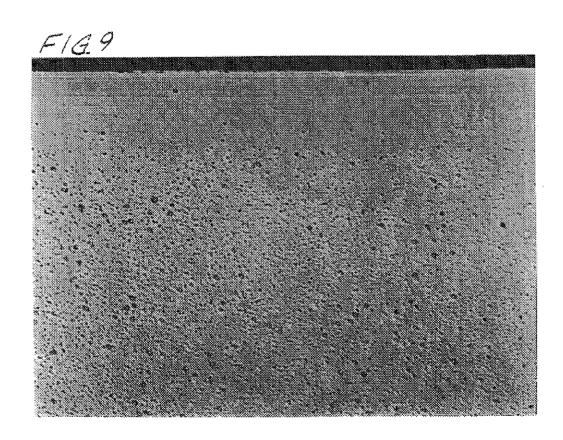


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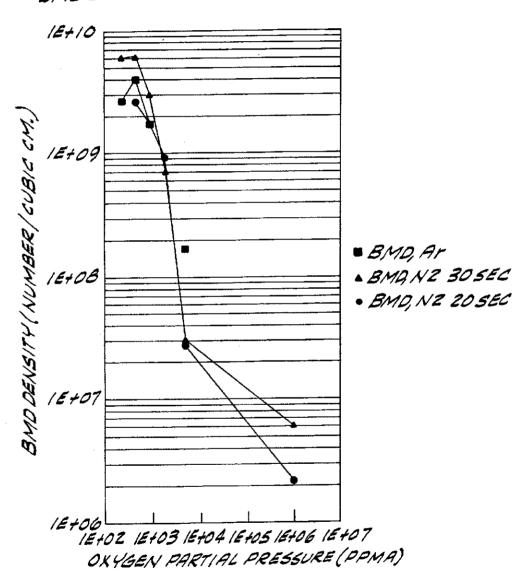
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FIG. 10 BMD DENSITY US. OXYGEN PARTIAL PRESSURE



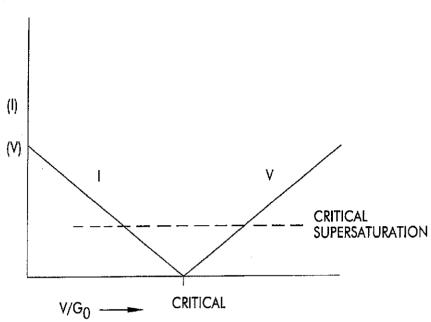
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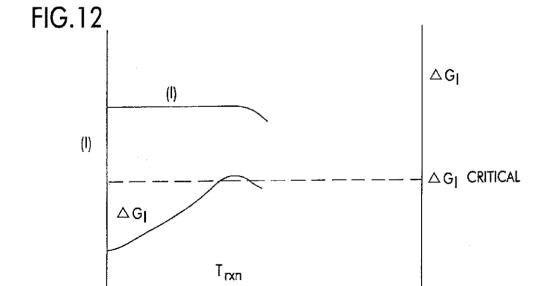
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FIG.11

~1400°C





-TEMP (C°) -

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FIG.13

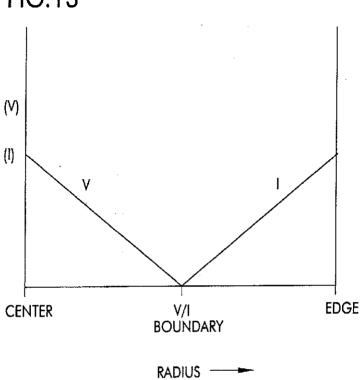
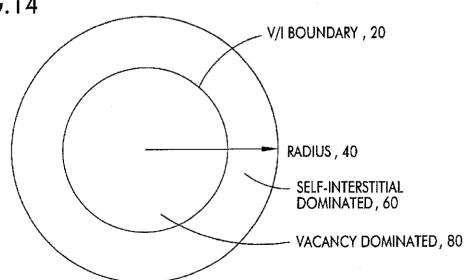
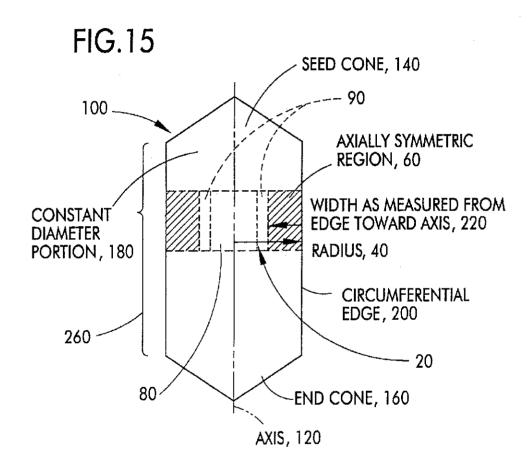


FIG.14



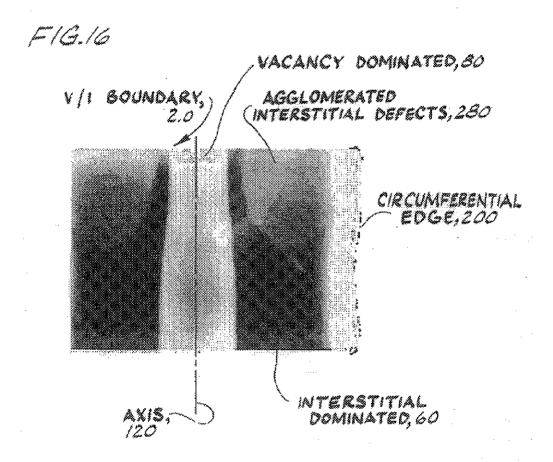
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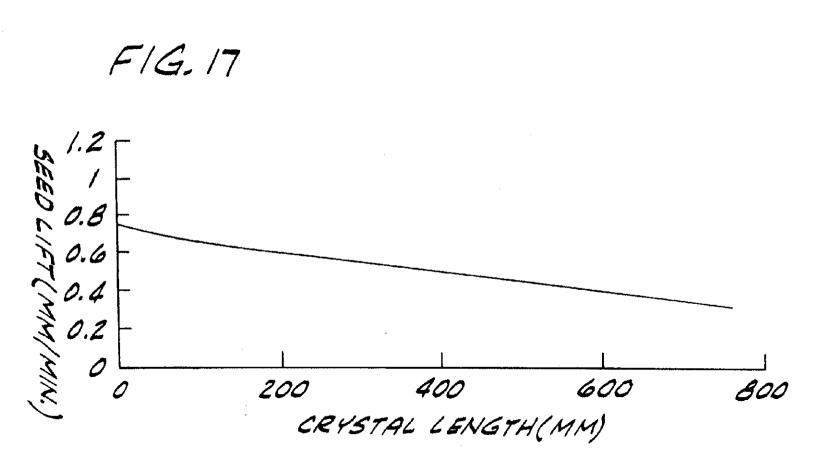
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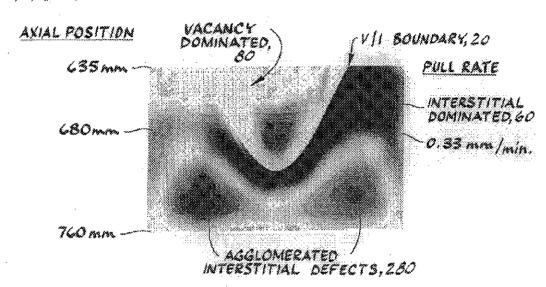


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